1. (Amended)

A context switching unit for switching a plurality of
contexts, the context switching unit comprising:

a register file having stored a context related to a thread
to be executed by an arithmetic logic unit or a memory access
unit, the register file comprising a read port, a write port,
a context-switching read port, and a context-switching write
port;

a context cache for caching a context, the context cache
comprising a read port and a write port, being connected
directly to the register file, and being contained in a central
processing unit in a on-chip manner;

a context switching bus for connecting the register file
and the context cache, the context switching bus comprising a
restore bus and a save bus for connecting the read port and the
write port of the context cache to the context-switching write
port and the context-switching read port of the register file
respectively; and

a thread control unit for controlling data transfer
between the context cache and the register file, the thread
control unit comprising a thread identifier table for storing
a thread identifier for identifying the context of a thread
stored in the context cache and being connected in parallel with
the arithmetic logic unit and the memory access unit,

wherein the thread control unit receives a context switch
instruction for executing a save operation and a restore
operation concurrently and the identifier of a new thread to
be interchanged, when a context switch which executes both a
context save operation and a context restore operation in
parallel occurs;

Art.34 Amendment

the thread control unit obtains a restore address where a new context to be interchanged is stored in the context cache and the save register identifier indicating the location where the current context is stored in the register file, by searching

5 through the thread identifier table in accordance with the thread identifier;

the thread control unit sends the obtained address to the context cache and sends the register identifier to the register file concurrently;

10 the register file, in accordance with the register identifier given by the thread control unit, outputs the data of the context to be saved from the context-switching read port and, concurrently writes the data of the context to be restored, sent from the read port of the context cache to the

15 context-switching write port through the restore bus, in the register corresponding to the register identifier;

the context cache, in accordance with the address given by the thread control unit, outputs the data of the context to be restored from the read port and, concurrently writes the data

20 of the context to be saved sent from the context-switching read port of the register file to the write port via the save bus; and

the context switching unit switches contexts by executing an operation for restoring a context from the context cache to

25 the register file and an operation for saving a context from the register file to the context cache concurrently.

2. (Amended)

A context switching unit according to Claim 1, wherein

30 the context switching bus has a bus width greater than the bit width of the register file.

Art.34 Amendment

3. (Amended)

A context switching unit according to Claim 1, wherein the thread control unit comprises as many thread identifier tables as required to identify contexts cached in the context
5   cache.

4. (Deleted)

5. A context switching unit according to any of Claims 1 to
10   4, wherein the thread control unit saves the context of the current thread from the register file to the context cache and sends the context of a new thread from the context cache to the register file concurrently to automatically interchange a required number of data items between the register file and the
15   context cache, when software, such as an operating system, issues a swap instruction for interchanging contexts, including a thread identifier as an operand, if the swap instruction is executed.

20   6. A context switching unit according to any of Claims 1 to 4, wherein the thread control unit transfers the data of a context from the register file to the context cache and does not transfer the data of a context from the context cache to the register file, when software, such as an operating system,
25   issues a backup instruction for saving a context, including a thread identifier as an operand, if the backup instruction is executed.

7. A context switching unit according to any of Claims 1 to
30   4, wherein the thread control unit transfers the data of a context from the context cache to the register file and does not transfer the data of a context from the register file to

the context cache, when software, such as an operating system, issues a restore instruction for restoring a context, including a thread identifier as an operand, if the restore instruction is executed.

5

8. A central processing unit comprising:

a context switching unit according to any of Claims 1 to 7;

an instruction cache for caching an instruction and a data

10   cache for caching data;

an instruction fetch unit for fetching an instruction from the instruction cache and decoding the instruction;

an arithmetic logic unit for performing an operation in accordance with an instruction stored in the register file and

15   writing the result of the operation back in the register file;

a memory access unit for receiving an operand and an instruction from the register file, accessing the data cache, and executing a load or store operation; and

an arithmetic bus for connecting the register file, the

20   arithmetic logic unit, the memory access unit, and the thread control unit in parallel.

9. A central processing unit according to Claim 8, wherein the memory access unit sends an address and data to the data cache

25   and stores the data in the data cache when a store instruction is given, and the memory access unit sends an address to the data cache, reads data from the data cache, and writes the read data back into the register file when a load instruction is given.

30

10. (Amended)

A context switching method for switching a plurality of

Art.34 Amendment

contexts by using a context switching unit comprising:

a register file having stored a context related to a thread to be executed by an arithmetic logic unit or a memory access unit, the register file comprising a read port, a write port, 5 a context-switching read port, and a context-switching write port;

a context cache for caching a context, the context cache comprising a read port and a write port, being connected directly to the register file, and being contained in a central 10 processing unit in a on-chip manner;

a context switching bus for connecting the register file and the context cache, the context switching bus comprising a restore bus and a save bus for connecting the read port and the write port of the context cache to the context-switching write 15 port and the context-switching read port of the register file respectively; and

a thread control unit for controlling data transfer between the context cache and the register file, the thread control unit comprising a thread identifier table for storing 20 a thread identifier for identifying the context of a thread stored in the context cache and being connected in parallel with the arithmetic logic unit and the memory access unit,

wherein the thread control unit receives a context switch instruction for executing a save operation and a restore 25 operation concurrently and the identifier of a new thread to be interchanged, when a context switch which executes both a context save operation and a context restore operation in parallel occurs;

the thread control unit obtains a restore address where 30 a new context to be interchanged is stored in the context cache and the save register identifier indicating the location where the current context is stored in the register file, by searching

through the thread identifier table in accordance with the thread identifier;

the thread control unit sends the obtained address to the context cache and sends the register identifier to the register file concurrently;

the register file, in accordance with the register identifier given by the thread control unit, outputs the data of the context to be saved from the context-switching read port and, concurrently writes the data of the context to be restored, sent from the read port of the context cache to the context-switching write port through the restore bus, in the register corresponding to the register identifier;

the context cache, in accordance with the address given by the thread control unit, outputs the data of the context to be restored from the read port and, concurrently writes the data of the context to be saved sent from the context-switching read port of the register file to the write port via the save bus; and

the context switching unit switches contexts by executing an operation for restoring a context from the context cache to the register file and an operation for saving a context from the register file to the context cache concurrently.

11. A context switching method according to Claim 10, saving the context of the current thread from the register file to the context cache and sending the context of a new thread from the context cache to the register file concurrently to automatically interchange a required number of data items between the register file and the context cache, when software, such as an operating system, issuing a swap instruction for interchanging contexts, including a thread identifier as an operand, if the swap instruction is executed.

Art.34 Amendment

12. A context switching method according to Claim 10, transferring the data of a context from the register file to the context cache and not transferring the data of a context from the context cache to the register file, when software, such as an operating system, issuing a backup instruction for saving a context, including a thread identifier as an operand, if the backup instruction is executed.

13. A context switching method according to Claim 10, transferring the data of a context from the context cache to the register file and not transferring the data of a context from the register file to the context cache, when software, such as an operating system, issuing a restore instruction for restoring a context, including a thread identifier as an operand, if the restore instruction is executed.

14. (Amended)

A context switching program for switching a plurality of contexts on a computer by using a context switching unit comprising:

a register file having stored a context related to a thread to be executed by an arithmetic logic unit or a memory access unit, the register file comprising a read port, a write port, a context-switching read port, and a context-switching write port;

a context cache for caching a context, the context cache comprising a read port and a write port, being connected directly to the register file, and being contained in a central processing unit in a on-chip manner;

a context switching bus for connecting the register file and the context cache, the context switching bus comprising a

restore bus and a save bus for connecting the read port and the write port of the context cache to the context-switching write port and the context-switching read port of the register file respectively; and

5   a thread control unit for controlling data transfer between the context cache and the register file, the thread control unit comprising a thread identifier table for storing a thread identifier for identifying the context of a thread stored in the context cache and being connected in parallel with

10 the arithmetic logic unit and the memory access unit,

   the context switching program for letting the computer execute:

   a step in which the thread control unit receives a context switch instruction for executing a save operation and a restore

15 operation concurrently and the identifier of a new thread to be interchanged, when a context switch which executes both a context save operation and a context restore operation in parallel occurs;

   a step in which the thread control unit obtains a restore

20 address where a new context to be interchanged is stored in the context cache and the save register identifier indicating the location where the current context is stored in the register file, by searching through the thread identifier table in accordance with the thread identifier;

25 a step in which the thread control unit sends the obtained address to the context cache and sends the register identifier to the register file concurrently;

   a step in which the register file, in accordance with the register identifier given by the thread control unit, outputs

30 the data of the context to be saved from the context-switching read port and, concurrently writes the data of the context to be restored, sent from the read port of the context cache to

the context-switching write port through the restore bus, in the register corresponding to the register identifier;

· a step in which the context cache, in accordance with the address given by the thread control unit, outputs the data of

5   the context to be restored from the read port and, concurrently writes the data of the context to be saved sent from the context-switching read port of the register file to the write port via the save bus; and

wherein the context switching unit switches contexts by

10   executing an operation for restoring a context from the context cache to the register file and an operation for saving a context from the register file to the context cache concurrently.

15. (Amended)

15   A computer-readable recording medium having recorded a context switching program for switching a plurality of contexts on a computer by using a context switching unit comprising:

a register file having stored a context related to a thread to be executed by an arithmetic logic unit or a memory access

20   unit, the register file comprising a read port, a write port, a context-switching read port, and a context-switching write port;

a context cache for caching a context, the context cache comprising a read port and a write port, being connected

25   directly to the register file, and being contained in a central processing unit in a on-chip manner;

a context switching bus for connecting the register file and the context cache, the context switching bus comprising a restore bus and a save bus for connecting the read port and the

30   write port of the context cache to the context-switching write port and the context-switching read port of the register file respectively; and

Art.34 Amendment

a thread control unit for controlling data transfer between the context cache and the register file, the thread control unit comprising a thread identifier table for storing a thread identifier for identifying the context of a thread

5 stored in the context cache and being connected in parallel with the arithmetic logic unit and the memory access unit,

the context switching program for letting the computer execute:

a step in wherein the thread control unit receives a

10 context switch instruction for executing a save operation and a restore operation concurrently and the identifier of a new thread to be interchanged, when a context switch which executes both a context save operation and a context restore operation in parallel occurs;

15 a step in which the thread control unit obtains a restore address where a new context to be interchanged is stored in the context cache and the save register identifier indicating the location where the current context is stored in the register file, by searching through the thread identifier table in

20 accordance with the thread identifier;

a step in which the thread control unit sends the obtained address to the context cache and sends the register identifier to the register file concurrently;

a step in which the register file, in accordance with the

25 register identifier given by the thread control unit, outputs the data of the context to be saved from the context-switching read port and, concurrently writes the data of the context to be restored, sent from the read port of the context cache to the context-switching write port through the restore bus, in

30 the register corresponding to the register identifier;

a step in which the context cache, in accordance with the address given by the thread control unit, outputs the data of

the context to be restored from the read port and, concurrently writes the data of the context to be saved sent from the context-switching read port of the register file to the write port via the save bus; and

5   wherein the context switching unit switches contexts by executing an operation for restoring a context from the context cache to the register file and an operation for saving a context from the register file to the context cache concurrently.